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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,838	03/17/2004	Naohiro Ueda	R2180.0193/P193	3147

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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,838	UEDA, NAOHIRO	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *11-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

1. Applicant's election without traverse of claims 1-10 in the reply filed on March 10, 2006 is acknowledged. Thereby, claims 11-16 are withdrawn from further consideration.

Claim Objections

2. Claims 1-10 are objected to because of the following informalities:

In line 6 of claim 1, the limitation "analog circuit" is unclear because applicant does not distinctly clarify what constitutes an "analog circuit." Does the input or output of the circuit have to be analog, or is any circuit with "a resistive element" considered an analog circuit? The office will interpret an analog circuit as any circuit that contains a resistive element. Claims 2-10 are dependent on claim 1, and thus contain the same error.

3. In line 2 of claim 4 and claim 6, the limitation, "the specific material of the resistive element," lacks antecedent basis. The office will interpret the specific material of claim 4 to be any material used to form a gate electrode. The office will interpret the specific material of claim 6 to be any material used to form an insulating film.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2 and 4-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kono et al. (US 5,972,756).

With respect to claim 1, Kono teaches (fig. 11) a semiconductor apparatus, comprising:

a semiconductor substrate **102** (col. 5, lns. 28-29);

an electrode pad **146** including a metal layer and formed on the semiconductor substrate (col. 6, lns. 56-58);

a MOS transistor **110a** formed on the semiconductor substrate (col. 5, lns. 55-59); and

an analog circuit **101a** (as best interpreted by the office) formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element **122 (123a, 123b)** including a semiconductor material (col. 6, lns. 11-15).

With respect to claim 2, Kono teaches a semiconductor apparatus as set forth in claim 1 above, wherein the resistive element **122** includes a specific material made of polysilicon **123a** (col. 6, lns. 13-14).

With respect to claim 4, Kono teaches a semiconductor apparatus as set forth in claim 1 above, wherein the MOS transistor **110a** comprises a gate electrode **109b**

including the specific material (as best interpreted by the office) of the resistive element (col. 5, lns. 56-57).

With respect to claim 5, Kono teaches a semiconductor apparatus as set forth in claim 1 above, further comprising:

an insulating film **124** formed on the semiconductor substrate **102** in a region in a vicinity of the electrode pad **146**; and

a fuse element **130** formed on the insulating film (col. 6, lns. 39-43).

With respect to claim 6, Kono teaches a semiconductor apparatus as set forth in claims 1 and 5 above, wherein the insulating film **124** includes the specific material (as best interpreted by the office) of the resistive element (col. 6, lns. 16-19).

With respect to claim 7, Kono teaches a semiconductor apparatus as set forth in claims 1 and 5 above, further comprising:

a rerouting layer **142b** formed in a region above the fuse element **130**; and

an external connection terminal **144** formed on the rerouting layer in a region different from a formation region of the electrode pad **146** (col. 6, lns. 53-56).

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Gris (US 6,806,536).

With respect to claim 1, Gris teaches (figs. 5-6) a semiconductor apparatus, comprising:

a semiconductor substrate **20** (col. 6, lns. 12-15);

an electrode pad **P2** including a metal layer **24** and formed on the semiconductor substrate (col. 6, lns. 21-23);

a MOS transistor formed on the semiconductor substrate (col. 7, lns. 37-42); and

an analog circuit (as best interpreted by the office) (fig. 7) formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element **R** including a semiconductor material (col. 7, lns. 57-59).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuniga et al. (US 2002/0000671) in view of Erdeljac et al. (US 5,489,547).

With respect to claim 1, Zuniga teaches (figs. 5-6) a semiconductor apparatus, comprising:

a semiconductor substrate **701** ();

an electrode pad **512** including a metal layer (fig. 5, "metal level II") and formed on the semiconductor substrate (pg. 5, [0051]);

a MOS transistor formed on the semiconductor substrate (pg. 5, [0052]); and

an analog circuit (as best understood by the office) formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element (pg. 5, [0052]).

Thus, Zuniga is shown to teach all the limitations of the claim with the exception of disclosing:

wherein the resistive element includes a semiconductor material.

However, Erdeljac teaches the fabrication of an integrated circuit device having polysilicon resistors (**32, 34, 56**) and MOS transistors (**44 and 50**) located under contacts **54** (fig. 11, col. 5, lns. 10-65). Thus, Erdeljac teaches an analog circuit (as best interpreted by the office) under a contact on a semiconductor substrate and comprising a resistive element (**32, 34, 56**) comprising a semiconductor material ("polysilicon").

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor apparatus of Zuniga to have a resistive element include a semiconductor material, such as polysilicon, as taught by Erdeljac, for the intended purpose of having an integrated circuit with precision polysilicon resistors, which are compatible with standard cell methodology and have a low temperature coefficient (col. 5, lns. 36-45).

With respect to claim 2, Erdeljac teaches wherein the resistive element includes a specific material made on polysilicon (col. 5, lns. 23-25).

With respect to claim 3, Erdeljac teaches wherein the resistive element includes a plurality of resistors (**32, 34, 56**) (col. 5, lns. 23-25).

With respect to claim 4, Erdeljac teaches wherein the MOS transistor comprises a gate electrode **24** including the specific material (as best interpreted by the office) of the resistive element (col. 2, lns. 5-6).

7. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kono '756 as applied to claims 1 and 5 above, and further in view of Tsuchida (US 6,232,823).

With respect to claim 8, Kono teaches the semiconductor apparatus as set forth in claims 1 and 5 above, with the exception of disclosing:

wherein the analog circuit comprises a voltage setting circuit, the resistive element comprises at least two resistors for producing a split voltage based on an input source power voltage, and the voltage setting circuit changes the split voltage according to a condition of the fuse element.

However, Tsuchida teaches voltage setting circuit (fig. 1), in which a resistive element comprises at least two resistors (**22, 23, 24, 25, 26**) for producing a split voltage based on an input source power voltage **21**, and the voltage setting circuit changes the split voltage according to a condition of the fuse element (**27, 28, 29, 30**) (col. 7, lns. 7-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor apparatus of Kono to include a voltage setting circuit, as taught by Tsuchida, for the disclosed intended purpose of providing a voltage setting circuit, in which the number of choices in the output voltage

is increased while suppressing the increase of an area occupied by resistors (col. 2, lns. 24-27).

With respect to claim 9, Tsuchida teaches a semiconductor apparatus as set forth claim 1 above, wherein the resistive element comprises at least two resistors (**22, 23, 24, 25, 26**) for producing a split voltage based on an input source power voltage, the analog circuit (fig. 6) comprises a reference voltage generator **51** for generating a reference voltage and a voltage detector including a comparator **52** for performing a comparison of the split voltage with the reference voltage (col. 11, lns. 50-67; col. 12, lns. 1-33).

With respect to claim 10, Tsuchida teaches a semiconductor apparatus as set forth claims 1 and 9 above, wherein the analog circuit (fig. 6) further comprises an output driver **54** for controlling an output voltage **55** based on an input voltage **53**, and the comparator **52** of the voltage detector outputs a gate control voltage ("operation voltage") as a result of the comparison for controlling the output driver to control the output voltage (col. 11, lns. 61-67; col. 12, lns. 1-5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AK
March 30, 2006

ANH D. MAI
PRIMARY EXAMINER